

Research Article

OV-CDMA System: Concept and Implementation

Elie Inaty and Rafic Ayoubi

*Department of Computer Engineering, Faculty of Engineering, University of Balamand, P.O. Box 100,
Deir El-Balamand, El-Koura, Lebanon*

Correspondence should be addressed to Elie Inaty, elie.inaty@balamand.edu.lb

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A new method is proposed to achieve a multirate overlapped code division multiple access system (OV-CDMA) based on a novel code overlapping procedure. The signal-to-interference ratio (SIR) performance has been investigated for such system. A channel model that allows multirate overlapped transmission is presented based on which a closed form solution for the SIR has been derived. In addition, a simple yet very efficient block diagram of the transmitter and the receiver architecture has been proposed for such a system. Based on the proposed block diagram, the encoder-decoder has been implemented using an FPGA. Numerical results show that the newly proposed OV-CDMA scheme outperforms the classical variable processing gain fast frequency hopping CDMA (VPG-FFH-CDMA) for different system scenarios. Finally, real-time measurements have been successfully obtained using a hardware prototype utilizing the simple Xilinx Spartan IIE (XC2S200E) FPGA.

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1. INTRODUCTION

During the past few years, there has been a growing interest in the development of broadband wireless communication networks for multimedia applications. The communication services in such networks can be high- and low-speed data, video, and many others with different performance and traffic requirements [1–3].

Classical fast frequency hopping CDMA (FFH-CDMA) has been discussed in many works [4–6]. A multirate FFH-CDMA system using variable processing gain (PG) (VPG-FFH-CDMA) has been proposed in [3, 7, 8]. The intention was to guarantee the one-to-one correspondence between the PG and the source transmission rate. The drawback of this system is the drastic decrease in the transmitted signal power especially for higher rate users for which the PG becomes very small. The solution to this problem is the use of power control [9]; on the other hand, Kwong and Yang in [7, 8] considered the multilength frequency hopping codes. Using these codes, rate and QoS are now dynamically matched to users' needs. The cutoff rate of the system is still limited by the physical constraints of the codes.

In this work, the general problem we considered is how much we can increase the transmission rates of different

classes of traffic beyond the nominal permitted rates. Our aim is to optimize performance to meet the quality of service (QoS) requirements given a fixed number of users in the network and a multimedia distribution. For an optimized family of codes, we will show that it is possible to increase a class bit rate beyond the nominal rate without decreasing the PG of the desired user or allowing any time delay between the data symbols. Our system achieves a multirate transmission by introducing an overlap between the transmitted symbols, hence the name overlapped code division multiple access system (OV-CDMA). In addition, we will consider the implementation of the OV-CDMA system [10]. The control unit of the transmitter and the receiver has been accomplished using FPGA. A pipeline technique is used to achieve a high-computational efficiency. A prototype is built and tested. We have been able to achieve a transmission rate ranging from 0.1 to 20 Mbps. It is imperative to mention that the five-channel case implemented in this paper can be easily modified to higher number of channels. This is the main advantage of FPGA [11].

The paper is organized as follows. In Section 2, we present the OV-CDMA encoding/decoding technique. Section 3 derives the performance of the OV-CDMA system. Section 4 describes the OV-CDMA system implementation

where the block diagrams of the transmitter and the receiver are presented and discussed. In addition, the hardware implementation using FPGA is discussed in Section 5. Section 6 contains the numerical results and the measurements. Finally, the conclusion is presented in Section 7.

2. OV-CDMA SYSTEM MODEL

Consider a multirate OV-CDMA communication system that supports M users in N different classes, which share the same medium [10]. The corresponding PGs for each class are given by $G_0 > G_1 > \dots > G_{N-1}$. The nominal bit duration is given by $T_s = G_s T_c$ with T_c being the chip duration. The corresponding nominal rate is $R_{n,s} = 1/T_s$. When the data rate increases beyond $R_{n,s}$, multibits can be coded during the time period T_s and transmitted together as revealed in Figure 1. In this figure, the PG is $G_s = 5$, which means that five channels are used in the coding process. When user k transmits using rate $R_s > R_{n,s}$, it introduces a bit overlap coefficient ε_s according to which the new rate is related to the nominal rate through the following:

$$R_s = \frac{G_s}{G_s - \varepsilon_s} R_{n,s}. \quad (1)$$

In Figure 1, the overlapping coefficient is $\varepsilon_s = 3$; therefore, the new transmission rate is $R_s = (5/2)R_{n,s}$. This means that the new transmission rate is 2.5 times the transmission rate without overlap. At a given receiver, the decoder observes practically multicode which is delayed according to the transmission rate of the source as shown in Figure 1.

In this paper, we assume the following: (1) a chip and bit synchronous system and a discrete rate variation, (2) all users in the class- s , $s \in \{0, 1, \dots, N-1\}$ have the same bit overlap coefficient $0 \leq \varepsilon_s < G_s - 1$; thus each class is characterized by (G_s, ε_s) , and (3) a unit transmission power for all the users.

2.1. Signal structure

We define $a_k^{(s)}(t, f)$ and $b_k^{(s)}(t)$ as the hopping pattern and the baseband signal, respectively, where t and f represent the time and frequency dimensions. From Figure 1, the bit stream can be seen to be serial-to-parallel converted to ν pulses. Assuming that the desired user is using the class- m , which is characterized by a PG G_m and an overlapping coefficient ε_m . Since the desired user nominal time period is $T_m = G_m T_c$, we are interested only in modeling the k th interfering channel during a time period T_m . Because the bit b_X^k from the ν -bits is delayed by $\tau_X = X(G_s - \varepsilon_s)T_c$, this suggests that the channel model, as seen by the desired receiver, can be represented as a tapped delay line with tap spacing of $\tau_{-1} = -(G_s - \varepsilon_s)T_c$ from left and $\tau_1 = (G_s - \varepsilon_s)T_c$ from right. The tap weight coefficients $b_X^k \in \{-1, 1\}$ depending on whether the transmitted bit is zero or one. The truncated tapped delay line model as seen by the desired receiver is shown in Figure 2. Accordingly, the transmitted signal is given by

$$S_k(t, f) = \sum_{\nu} b_{\nu}^k a_k^{(s)}(t - \tau_{\nu}, f). \quad (2)$$

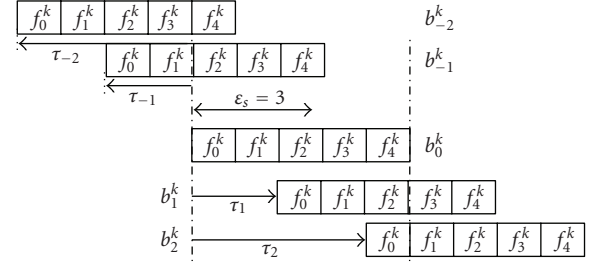


FIGURE 1: Coding method of the proposed OV-CDMA system with $G_s = 5$ and $\varepsilon_s = 3$.

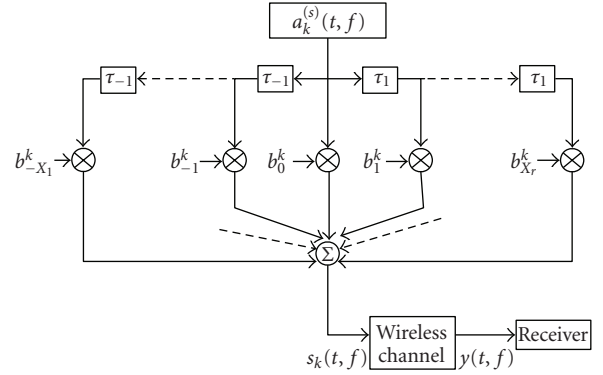


FIGURE 2: OV-CDMA channel model.

Lemma 1. Given an interferer k with (G_s, ε_s) and the desired user with (G_m, ε_m) for all $s, m \in \{0, 1, \dots, N-1\}$. At the desired receiver end, during the nominal time period T_m , the observed total number of taps in channel k is given by

$$N_k(G_m, G_s, \varepsilon_s) = \left\lfloor \frac{\varepsilon_s}{G_s - \varepsilon_s} \right\rfloor + \left\lfloor \frac{\Delta G + \varepsilon_s}{G_s - \varepsilon_s} \right\rfloor + 1, \quad (3)$$

where $\Delta G = G_m - G_s$.

Lemma 2. Given an interferer k with (G_s, ε_s) and the desired user with (G_m, ε_m) , the observed total number of transmitted codes from transmitter k that undergo a total overlap with the desired correlator during T_m and excluding the normal bit b_0^k is given by

$$X_t = \left\lfloor \frac{|\Delta G|}{G_s - \varepsilon_s} \right\rfloor, \quad (4)$$

where $\lfloor x \rfloor$ is the highest integer smaller than x and $|\Delta G|$ is given by

$$|\Delta G| = \begin{cases} G_m - G_s, & \text{if } G_m > G_s, \\ G_s - G_m, & \text{if } G_m \leq G_s. \end{cases} \quad (5)$$

The received signal at the input of the decoder is therefore given by

$$y(t, f) = n(t) + \sum_{k=0}^{M-1} \sum_{\nu=-X_l}^{X_r} b_{\nu}^k a_k^{(s)}(t - \tau_{\nu}, f), \quad (6)$$

where $n(t)$ is an additive white Gaussian noise (AWGN) with two-sided power spectral density $\Gamma_0/2$.

2.2. Decoder's output

Without loss of generality, we assume that the correlation-matched filter is matched to the zeroth signal with class- m . The output of the matched filter correlator will be

$$Z_0^{(m)} = \Gamma + \int_0^{T_m} \sum_{k=0}^{M-1} S_k(t - \tau_v, f) a_0^{(m)}(t, f) dt, \quad (7)$$

where Γ is a zero-mean AWGN with variance $\sigma_n^2 = \Gamma T_m/4$. The multiple access interference (MAI) I_k from user k that transmits data with rate R_s can be written as

$$\begin{aligned} I_k &= \sum_{v=-X_l}^{-1} \int_0^{\tau_v} b_v^k h(a_k^{(s)}(t - \tau_v), a_0^{(m)}(t)) dt \\ &\quad + \sum_{v=0}^{X_l} \int_{\tau_v}^{\tau_v + T_s} b_v^k h(a_k^{(s)}(t - \tau_v), a_0^{(m)}(t)) dt \\ &\quad + \sum_{v=X_l+1}^{X_r} \int_{\tau_v}^{T_m} b_v^k h(a_k^{(s)}(t - \tau_v), a_0^{(m)}(t)) dt, \quad G_m > G_s, \\ I_k &= \sum_{v=-X_l}^{1-X_l} \int_0^{\tau_v} b_v^k h(a_k^{(s)}(t - \tau_v), a_0^{(m)}(t)) dt \\ &\quad + \sum_{v=-X_l}^0 \int_0^{T_m} b_v^k h(a_k^{(s)}(t - \tau_v), a_0^{(m)}(t)) dt \\ &\quad + \sum_{v=1}^{X_r} \int_{\tau_v}^{T_m} b_v^k h(a_k^{(s)}(t - \tau_v), a_0^{(m)}(t)) dt, \quad G_m \leq G_s, \end{aligned} \quad (8)$$

for all $k \neq 0$. $h(\cdot)$ is the Hamming function [10]. The sequences $a_k^{(s)}(t)$ and $a_0^{(m)}(t)$ are numbers representing frequencies used at time t for the k th interferer and the desired user, respectively. Notice that $a_k^{(s)}(i) = a_k^{(s)}(i + T_s)$. In addition, we define a new performance parameter called the auto-interference I_0 caused by the desired user's signal and it is given by

$$\begin{aligned} I_0 &= \sum_{v=-X_r}^{-1} \int_0^{\tau_v} b_v^0 h(a_0^{(m)}(t - \tau_v), a_0^{(m)}(t)) dt \\ &\quad + \sum_{v=1}^{X_r} \int_{\tau_v}^{T_m} b_v^0 h(a_0^{(m)}(t - \tau_v), a_0^{(m)}(t)) dt. \end{aligned} \quad (9)$$

3. OV-CDMA PERFORMANCE EVALUATION

Since the user may set a connection for a particular multimedia class and modify it dynamically, the index s is a discrete random variable with a certain prior probability

$$\begin{aligned} p_k^{(i)} &= \Pr(\text{user } k \text{ chooses class-} i) \\ &= \Pr(s = i) \quad \forall i \in \{0, 1, \dots, N-1\} \end{aligned} \quad (10)$$

with $\sum_{s=0}^{N-1} p_k^{(s)} = 1$ and we call $p_k^{(s)}$ the multimedia probability mass function (pmf) for user k . I_k , for all $0 \leq k \leq M-1$,

is assumed to be an independent random variable. Hence the variance of the decision variable $Z_0^{(m)}$ is

$$\text{var}[Z_0^{(m)}] = \sum_{k=1}^{M-1} \sum_{s=0}^{N-1} p_k^{(s)} \sigma_{I_{k/s}}^2 + \sigma_{I_0}^2 + \sigma_n^2, \quad (11)$$

$\sigma_{I_{k/s}}^2$ and $\sigma_{I_0}^2$ represent the interference power caused by an active user k using class- s and the auto-interference power caused by the desired user due to overlapping, respectively, and they are given by

$$\begin{aligned} \sigma_{I_{k/s}}^2 &= E\left(\frac{I_k^2}{s}\right) - E^2\left(\frac{I_k}{s}\right), \\ \sigma_{I_0}^2 &= E(I_0^2) - E^2(I_0), \end{aligned} \quad (12)$$

where $E(\cdot)$ is the expectation operator over all possible values of the overlapping bits b_X^k for $X \in \{-X_l, \dots, X_r\}$ assuming that $\Pr(b_X^k = 1) = \Pr(b_X^k = -1) = 1/2$. $E(I_k/s)$ and the cross terms generated from squaring the summation in $E(I_k^2/s)$ become zeros because the average over the bit is zero, which enables us to write

$$\begin{aligned} E\left(\frac{I_k^2}{s}\right) &= R_k(T_m, T_s, \epsilon_s) \\ &= \begin{cases} \frac{1}{2} \left[\sum_{v=-X_l}^{-1} H_{k,0}^2(0, \tau_v) + \sum_{v=0}^{X_l} H_{k,0}^2(\tau_v, \tau_v + T_s) \right. \\ \quad \left. + \sum_{v=X_l+1}^{X_r} H_{k,0}^2(\tau_v, T_m) \right], & G_m > G_s, \\ \frac{1}{2} \left[\sum_{v=-X_l}^{1-X_l} H_{k,0}^2(0, \tau_v) + \sum_{v=-X_l}^0 H_{k,0}^2(0, T_m) \right. \\ \quad \left. + \sum_{v=1}^{X_r} H_{k,0}^2(\tau_v, T_m) \right], & G_m \leq G_s, \end{cases} \end{aligned} \quad (13)$$

$$\begin{aligned} E(I_0^2) &= R_0(T_m, \epsilon_m) \\ &= \frac{1}{2} \left[\sum_{v=-X_r}^{-1} H_{0,0}^2(0, \tau_v) + \sum_{v=1}^{X_r} H_{0,0}^2(\tau_v, T_m) \right], \end{aligned} \quad (14)$$

where

$$H_{k,0}(\tau_i, \tau_j) = \int_{\tau_i}^{\tau_j} h(a_k(t - \tau_v), a_0(t)) dt. \quad (15)$$

Let $q_v = \tau_v/T_c$, we can write

$$\begin{aligned} H_{k,0}(0, \tau_v) &= T_c H_v(0, q_v) = T_c \sum_{j=0}^{q_v-1} h(a_{j-q_v}^k, a_j^0), \\ H_{k,0}(\tau_v, T_m) &= T_c H_v(q_v, G_m) = T_c \sum_{j=q_v}^{G_m-1} h(a_{j-q_v}^k, a_j^0), \\ H_{k,0}(\tau_v, \tau_v + T_s) &= T_c H_v(q_v, q_v + G_s) = T_c \sum_{j=q_v}^{q_v+G_s-1} h(a_{j-q_v}^k, a_j^0). \end{aligned} \quad (16)$$

If we define $R_k(G_m, G_s, \varepsilon_s) = R_k(T_m, T_s, \varepsilon_s)/(T_c^2/2)$ and $R_0(G_m, \varepsilon_m) = R_0(T_m, \varepsilon_m)/(T_c^2/2)$, then we substitute into (12), the SIR experienced by any active user that uses class- m is

$$SIR_m = \frac{\alpha^2 G_m^2}{\sum_{k=1}^{M-1} \sum_{s=0}^{N-1} p_k^{(s)} R_k(G_m, G_s, \varepsilon_s) + R_0(G_m, \varepsilon_m) + \sigma_n^2}, \quad (17)$$

where α is a random variable with a Rayleigh distribution assuming a Rayleigh fading channel. Thus the distribution of α^2 is exponential [12].

3.1. Effective increase in the number of hits

Proposition 1. *For one-coincidence sequences with nonrepeating frequencies [13, 14], the expected value of the increase in the number of hits caused by any active interferer with (G_s, ε_s) on a desired user with (G_m, ε_m) is given by (19). In addition, the effective increase of the number of hits due to the auto-interference is*

$$I_H^0(G_m, \varepsilon_m) = 0, \quad (18)$$

where X_r, X_l, X_t , and $|\Delta G|$ are given throughout Lemmas 1 and 2, and F is the total number of available frequencies,

$$I_H^k(G_m, G_s, \varepsilon_s) = \frac{1}{F} \left[\left(G_s - \frac{(G_s - \varepsilon_s)}{2} \right) X_l - \frac{(G_s - \varepsilon_s)}{2} X_l^2 + \left(G_m - \frac{(G_s - \varepsilon_s)}{2} \right) X_r - \frac{(G_s - \varepsilon_s)}{2} X_r^2 + \left(\frac{(G_s - \varepsilon_s)}{2} - |\Delta G| \right) X_t + \frac{(G_s - \varepsilon_s)}{2} X_t^2 \right]. \quad (19)$$

3.2. Average SIR

Assuming that the overlapping codes are independent virtual active users and one-coincidence sequences, we can compute the average correlations given in (13). In addition, if we assume that the multimedia pmf is the same for every user, $p_k^{(s)} = p^{(s)}$, the average SIR for the desired user with (G_m, ε_m) will be

$$SIR_m = \frac{\alpha^2 G_m^2}{((M-1)/2)\beta + \sigma_n^2}, \quad (20)$$

where $\beta = \{ \sum_{s=0}^{N-1} ([p^{(s)} \cdot G_s]/F) + \sum_{s=0}^{N-1} [p^{(s)} \cdot I_H^k(G_m, G_s, \varepsilon_s)] \}$. In (20), we have been able to separate the interference power into the normal MAI power caused by active users when $R_s = R_{n,s}$ and the one caused by virtual users that overlap with the desired user's code when $R_s > R_{n,s}$.

4. OV-CDMA SYSTEM IMPLEMENTATION

Throughout this paper, and without loss of generality, the analysis is based on the five-channel example presented in Figure 1. The problem of designing a transmitter that performs the overlapping operation is simplified to find a

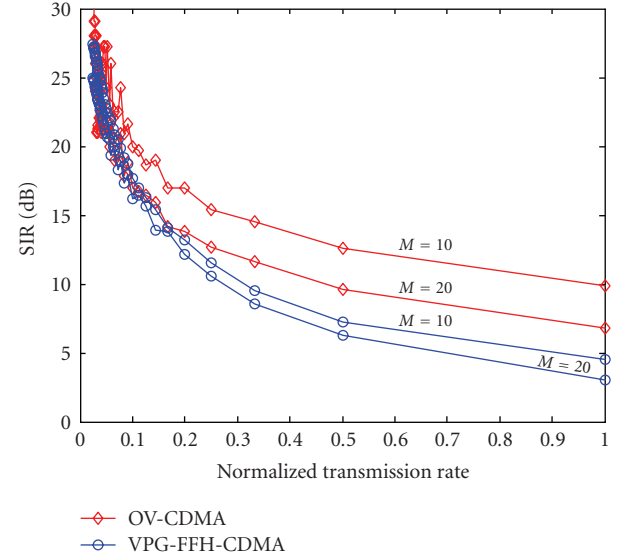


FIGURE 3: Average SIR versus the normalized transmission rate.

way to transmit more than one frequency channels during the same chip period T_c as shown in Figure 1.

4.1. OV-CDMA transmitter implementation

For example, during the first period T_c , the transmitter should send channels f_0^k, f_2^k , and f_4^k at the same time. Classical FFH-CDMA transmitters use what is widely known as frequency synthesizer to generate one carrier frequency at each T_c seconds. It cannot generate multifrequency at the same time. For this reason, we propose a new architecture based on multifrequency generators and a switching operation that is performed by a central processing unit as revealed by Figure 4(a). The control unit will determine the switches which must be closed and the other which should be open. The result is summed and transmitted. This task can be easily accomplished using the desired user's code as shown in Figure 4(b). The above five-by-five matrix of binary data represents the digital control code that must be used by the control unit for the five-channel example shown in Figure 1. Note that during the first chip duration, the switches are controlled by the first row of the matrix such that S_1, S_3 , and S_5 are closed, and S_2 and S_4 are open. This enables us to transmit simultaneously channels f_0^k, f_2^k , and f_4^k . This matrix will be repeated every bit duration T_n .

4.2. OV-CDMA receiver implementation

The receiver should first perform the decoding operation of the overlapped code then decide whether the transmitted bit is zero or one. The block diagram of the receiver is shown in Figure 5. It is composed of two major parts: the analog part and the digital part using FPGA. In the analog circuitry part, the incoming radio frequency signal is detected using the CDM2502 antenna. The incoming electric signal is subdivided into five channels with equal power. Then, for every channel, a bandpass filter (BPF) is used with a center

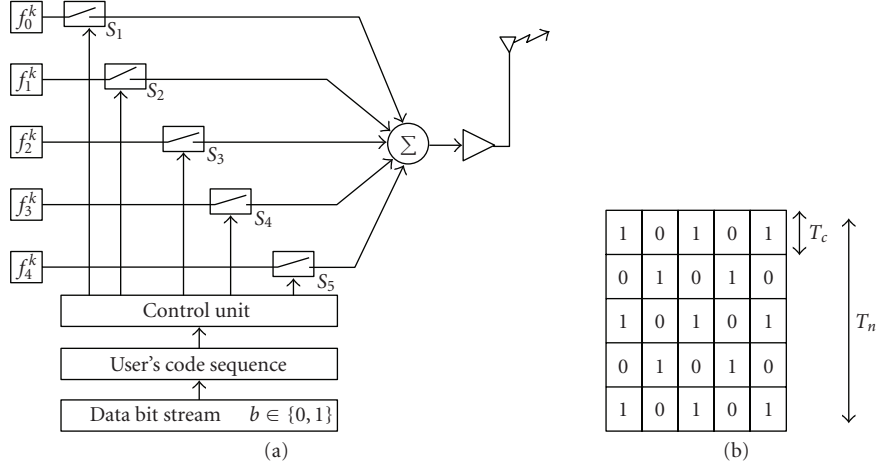


FIGURE 4: (a) Five-channel OV-CDMA transmitter, (b) OV-CDMA digital control unit.

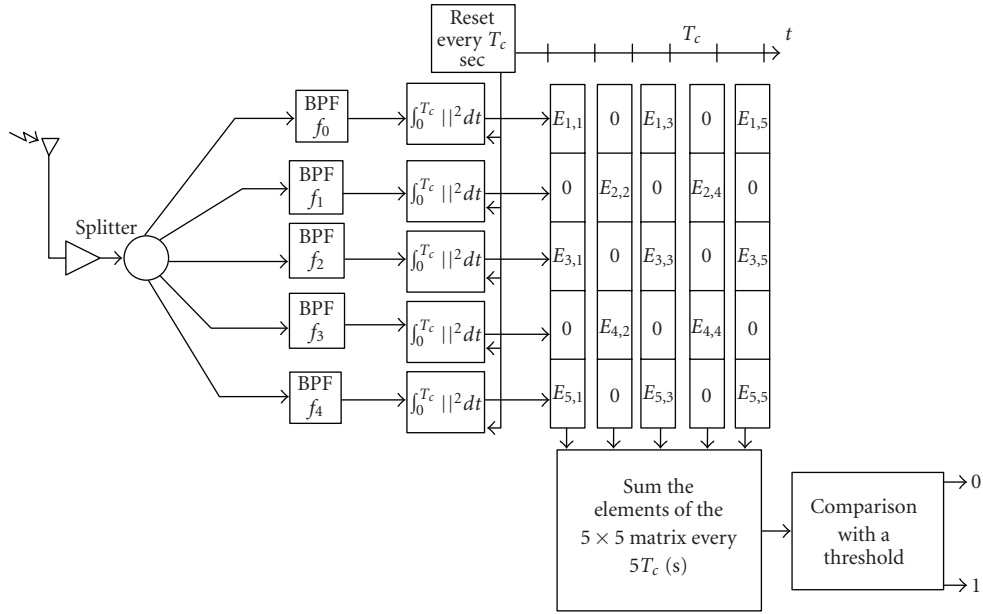


FIGURE 5: Five-channel OV-CDMA receiver.

frequency f_i^k , which is one of the employed channels by the desired user. An energy detector (ED) is used to measure the energy of the filtered signal. An analog-to-digital converter (ADC) is utilized in order to convert the analog information from the ED into digital one so that it can be accepted by the FPGA logic.

It is imperative to mention that we will use the same code logic used in the encoder side. This code replica is used to disperse the received signal and to obtain the transmitted data stream. The outputs of the ADCs are held inside the registers then shifted to the right at every time period T_c . After five consecutive cycles, a 5×5 matrix is constructed. The contents of this matrix are added, then the result is compared to a predefined detection threshold. The compared data is the energy added after five consecutive

cycles. If the result is less than the threshold, it is estimated that 0 is transmitted; otherwise, it is judged that 1 is sent.

5. DIGITAL IMPLEMENTATION USING FPGA

After data is received, it is digitally processed using FPGA technology. The target FPGA family is a Xilinx Spartan IIE (XC2S200E) due to the availability of boards based on this family in our labs. In order to achieve high performance, pipelining technique was used. A block diagram of the FPGA implementation is shown in Figure 6. Even though the figure shows an example of eight channels, only five channels were implemented in hardware. However, our implementation can be generalized to any number of channels.

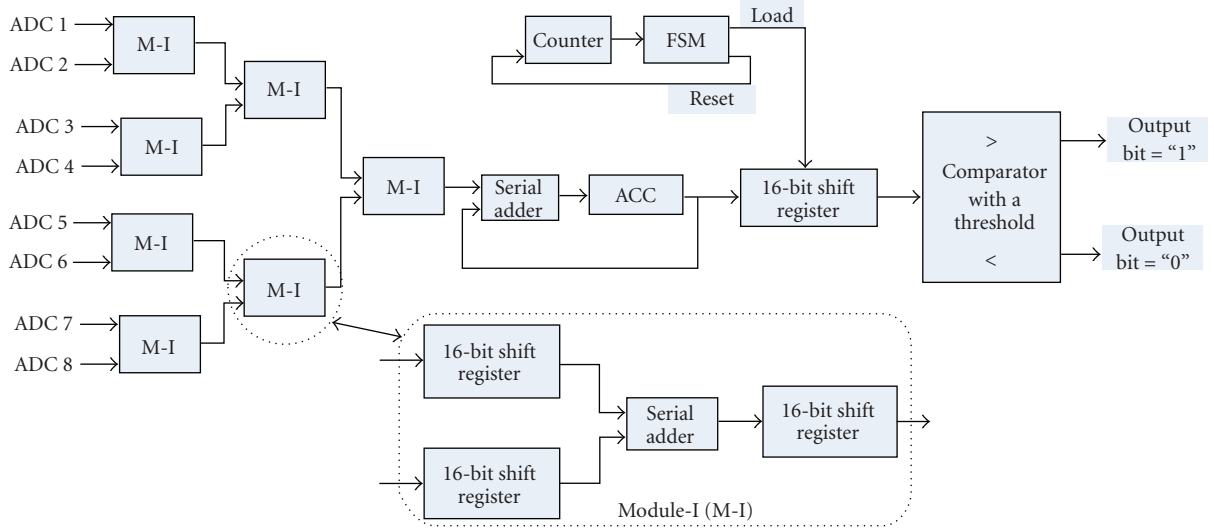


FIGURE 6: Logic block diagram of the decoder and the decision of the receiver.

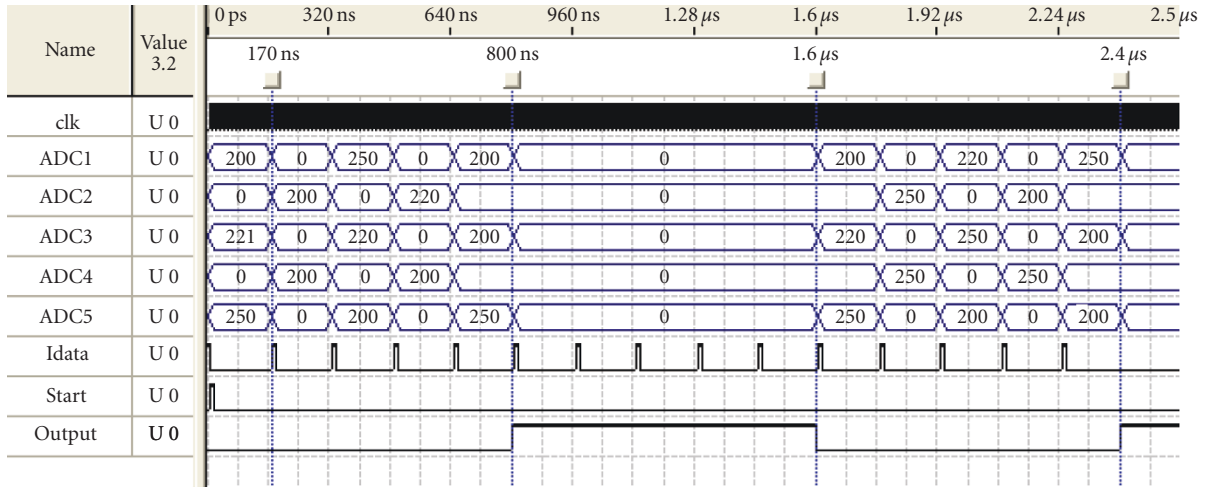


FIGURE 7: Simulated timing diagram.

For an N -channel receiver, an $N \times N$ addition is required every bit period T_n , which is composed of N chip periods T_c ; in addition, each T_c seconds is composed of 16-bit stream. The addition is performed in a tree fashion (see Figure 6). Therefore, it takes $\log_2(N)$ cycles to sum N numbers (N channels). Since we need $N \times N$ addition, the summation should be performed N times; that is $N \log_2(N)$ cycles. However, by using pipelining technique, we were able to reduce the number of cycles for an $N \times N$ addition to $\log_2(N) + (N - 1)$.

This high-speed implementation is achieved at the expense of $N - 1$ adders. In order to reduce the area occupied by the design, serial adders were used. Even though the summation of 16-by-16 bits requires 16 cycles, the clock frequency achieved is several times higher than that of a parallel adder.

As an example, consider an 8-channel receiver (Figure 6). Every chip period T_c eight 8-bit ADCs convert the received

analog signals into eight bits, which are extended into 16 bits and shifted serially into eight 16-bit shift registers. The serial outputs from every two shift registers are fed into a serial adder, which will perform the summation and generate the sum of one bit at a time. The output of each adder is connected to the input of another 16-bit shift register in order to store the results of the summation. Each module (M-I) in Figure 6 corresponds to two shift registers at the input of an adder and another shift register connected to the output of the adder.

For this eight channels example, the proposed implementation consists of a three-stage pipeline that performs the addition in a tree fashion. After initially filling the pipeline stages (this requires 3 clock cycles), all pipeline stages will be performing similar tasks. For instance, every clock cycle, Stage 1 would be performing four summations on the newly received data from the ADCs, whereas Stage 2 would be doing two parallel summations on the already summed data

TABLE 1: Implementation results.

Number of slices	138 out of 2352 5%
Number of slice flip flops	232 out of 4704 4%
Number of 4 input LUTs	86 out of 4704 1%
Max. clock frequency	100.675 MHz

from Stage 1 that corresponds to the older ADC conversion. At the same time, Stage 3 would be summing the results from Stage 2 of the previous data. After eight clock cycles, an output bit is generated based on a threshold comparison, and the accumulator register is cleared in order to start accumulating data for a new output bit. This process is repeated after each eight clock cycles.

Table 1 summarizes the mapping results in terms of logical resources and maximal clock period on a Xilinx Spartan IIE XC2S200E speed grade-7 FPGA. As shown in Table 1, for our 5-channel receiver, the utilization of the FPGA chip did not exceed 5%, which means that we can easily upgrade our design into cases including larger number of channels on the same Spartan IIE used. Moreover, the clock period achieved was less than 10 nanoseconds.

6. NUMERICAL RESULTS AND MEASUREMENTS

For the purpose of comparing the performance of our newly proposed OV-CDMA system with existing multirate systems, Figure 3 shows the SIR comparison between the OV-CDMA and the classical VPG-FFH-CDMA systems while varying the transmission rate. The transmission rate is normalized in the sense that it begins by zero when $\epsilon_s = 0$ for the OV-CDMA system and when $G_s = 40$ for the VPG FFH-CDMA system. The normalized transmission rate increases by increasing ϵ_s or decreasing G_s for the OV-CDMA and the VPG-FFH-CDMA, respectively. Notice that, for either $M = 10$ or $M = 20$ users, the SIR for the OV-CDMA system is always greater than that of the VPG-FFH-CDMA system.

In Figure 7, we present the simulated timing diagram for the OV-CDMA receiver in which the input signals ADC1, ADC2, ADC3, ADC4, and ADC5 to the FPGA are coming from the ADCs. This simulation is performed for an overlapping coefficient $\epsilon_s = 3$. Each input is composed of eight parallel bits. Each output bit lasts for the whole period of five data reception, after which the new bit is output based on the last five data reception. The optimal detection threshold is obtained using the maximum likelihood detection scheme. After comparison with the threshold, the decision for the possible transmitted symbol is shown in *Output*.

The test bed has been implemented using an educational FPGA board which is the Xilinx Spartan IIE XC2S200E speed grade-7. In addition, the setup includes a wireless local area network antenna of type CDM2502 working in the 2.4-2.5 GHz band. Using this test bed, we have been able to transmit and receive a digital signal successfully. Figures 8(a) and 8(c) show the transmitted and the corresponding measured received information signals, respectively, in the presence of three interferers and using the five channels encoder-decoder presented previously. The results show clearly that the

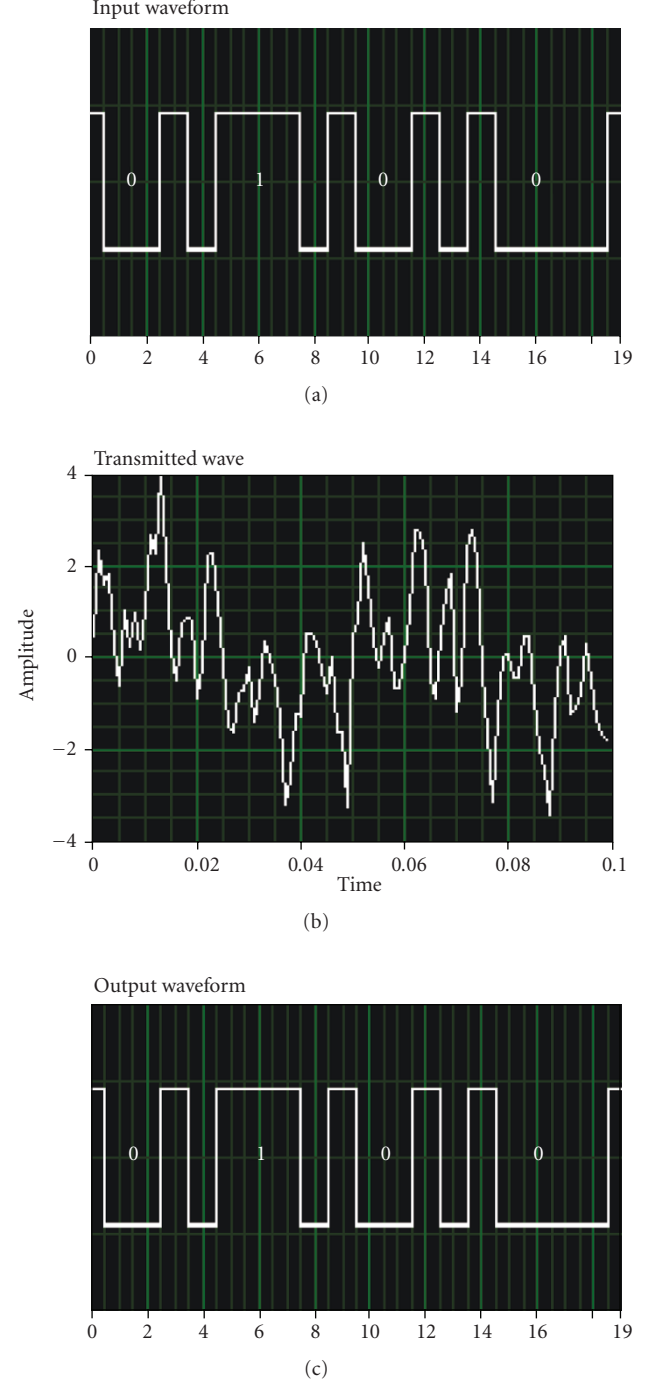


FIGURE 8: Measured signals: (a) binary input wave, (b) OV-CDMA coded signal, and (c) binary-decoded wave.

three transmitted bits are received successfully. In addition, Figure 8(b) is the measured OV-CDMA coded transmitted signal of the desired user.

Using the test bed built in our labs, we have been able to measure the SIR and the bit error rate (BER) of our proposed system. An experiment has been conducted using a very high number of coded bits using our technique. Figure 9

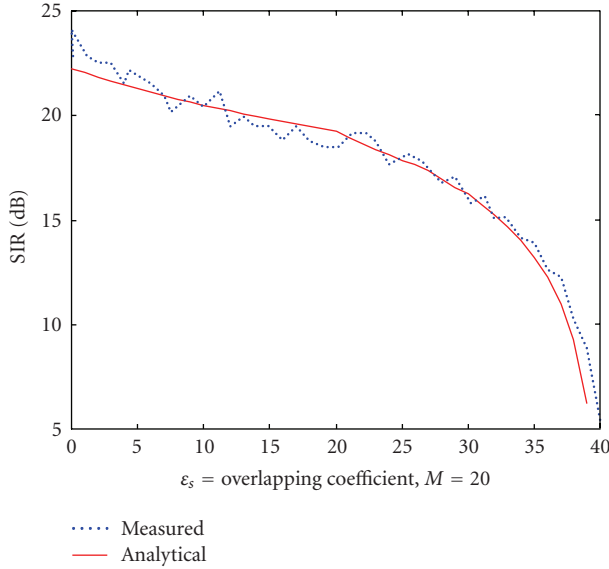


FIGURE 9: System's SIR (in dB) versus the overlapping coefficient using real measurements and the analytical results obtained in (20).

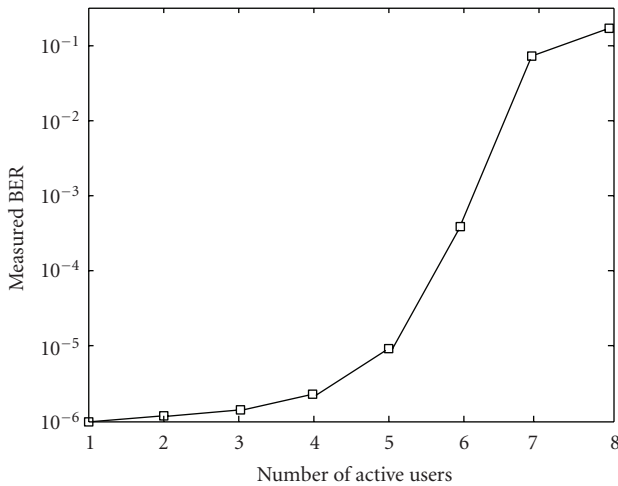


FIGURE 10: Measured bit error rate.

shows the measured SIR and the simulated one using the derived equation in (17) versus the overlapping coefficient. We assume 20 active terminals. It is clear that there is a total agreement between the measured and the analytical results. On the other hand, using a transmission rate of 10 Mbits/s, Figure 10 presents measured BER versus the total number of active simultaneous users in the network. It is clear that our system guarantees a good performance in the presence of MAI.

7. CONCLUSION

In this paper, we have proposed a simple technique yet very efficient to implement a multirate/multiclass CDMA system based on a novel code overlapping procedure. A system model was presented and the SIR was derived. The

block diagram of the transmitter and the receiver were presented and discussed. Moreover, an efficient FPGA-based transceiver implementation was shown. This implementation was efficient in terms of both speed and area. Using simple educational FPGA board of type Xilinx Spartan IIE (XC2S200E), the measurement results showed that the proposed system can achieve very good performance in the presence of MAI. Both simulation and measurements showed that it is possible to increase the transmission rate well beyond the nominal rate. On the other hand, simulation results reveal that our newly proposed OV-CDMA outperform the classical VPG-FFH-CDMA.

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